Half Adder

Half adder is used to add two digit numbers and it will give us output of sum and carry

**TRUTH TABLE:**

| **INPUT**  **A** | **INPUT** | **OUTPUT**  **CARRY** | **OUTPUT**  **CARRY** |
| --- | --- | --- | --- |
| 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 0 |

Half adder is basically constructed by using an **EX-OR** gate and **AND** gate

**VERILOG CODE :**

// Half adder code using Data Flow modelling

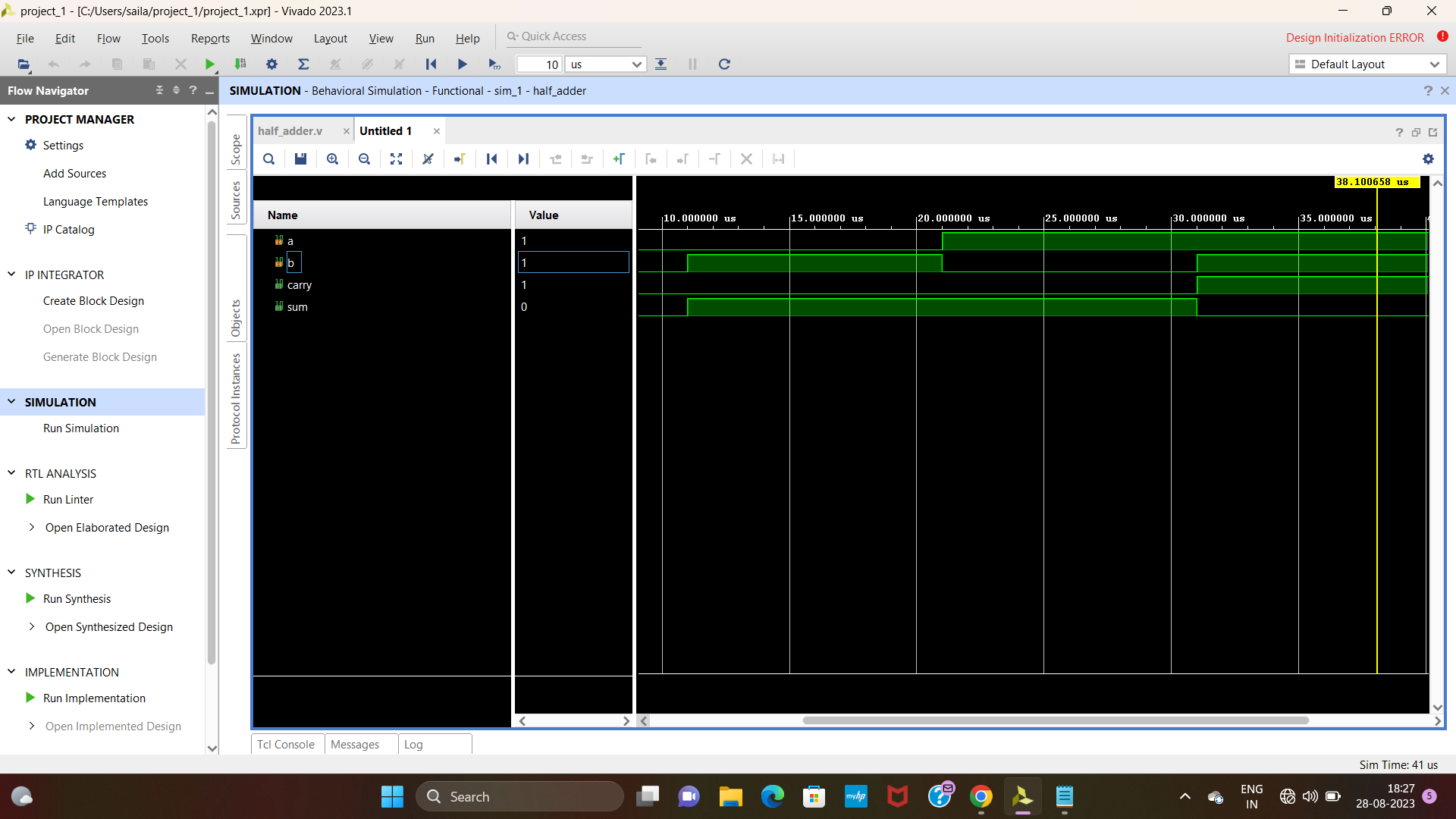
module half\_adder( input a,b , output carry,sum);

assign sum = a^b;

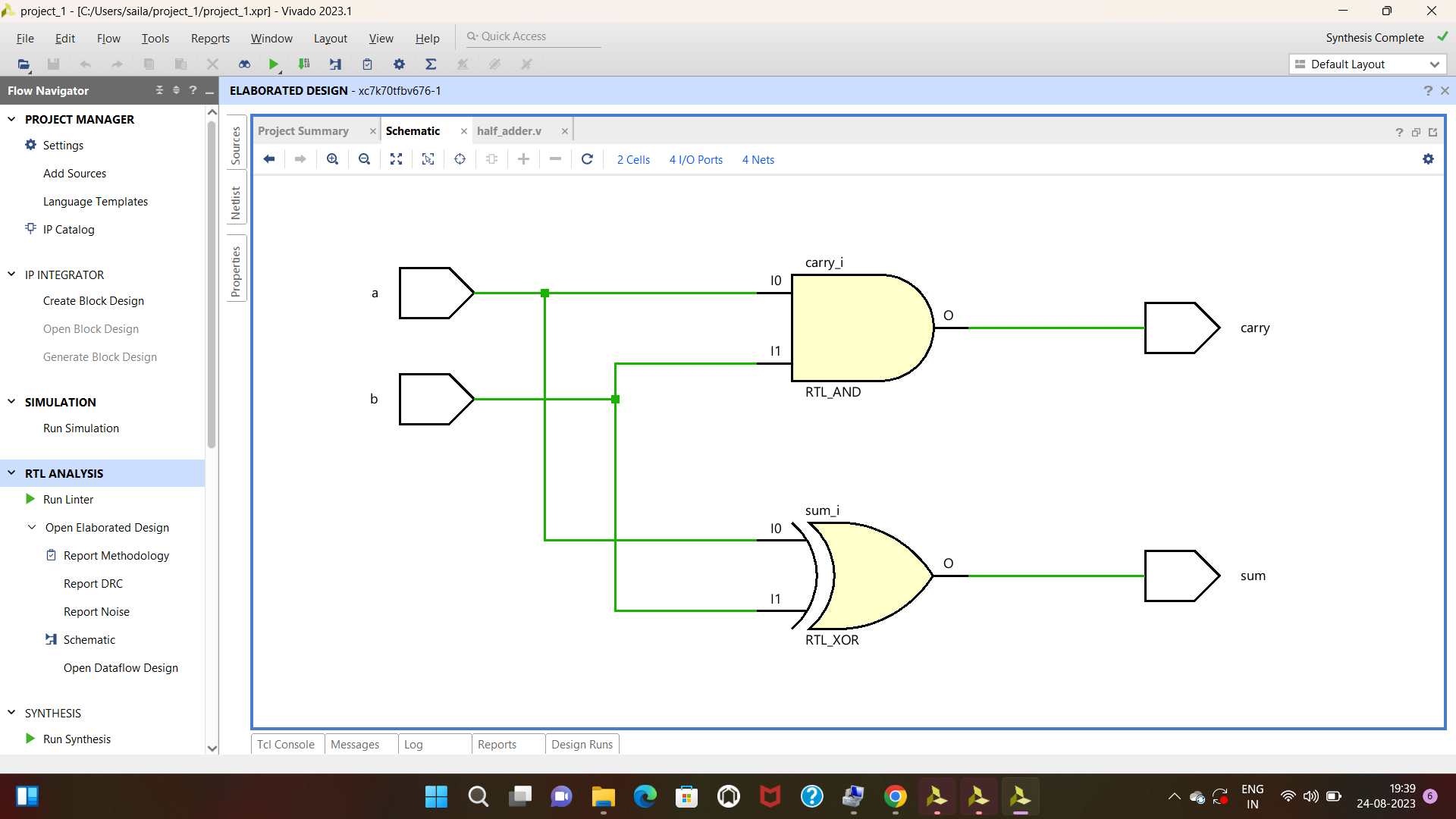
assign carry= a&b;

endmodule

**SIMULATION OUTPUT:**



**SCHEMATIC DIAGRAM:**

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